UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,147	12/03/2003	Saverio Pezzini	02AG33853417	5293

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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/727,147	PEZZINI, SAVERIO
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-38* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-19,22-26,29-31,34,35 and 38* is/are rejected.

7)☒ Claim(s) *20,21,27,28,32,33,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/3/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claims 15-19, 22-26, 29-31, 34-35, 38 are rejected under 35 U.S.C. 102(e) as

being anticipated by Moyer et al. (US Patent 6,449,676)

As per claim 15, Moyer discloses a computer system comprising:

at least one peripheral (fig.2, 50 ie interrupt sources) for generating

interrupt requests;(col.3, lines 40-61)

an interrupt pending register(fig.2, 58 ie interrupt pending register) for

storing the interrupt request; (col.3, lines 15-61)

a microprocessor(fig.2, 12 ie cpu) for processing interrupts;(col.3, lines 15-

61)

an interrupt control circuit(fig.2, 81 ie Oring circuit) coupled to said

interrupt pending register and said microprocessor for providing an interrupt

command to said microprocessor based upon the stored interrupt requests; and

(col.4, line 43-col.5, line 47)

an auxiliary interrupt control circuit(fig.2, 10 ie data processing system)

coupled to said at least one peripheral and said microprocessor for generating a

bit string identifying an active bit stored in the interrupt pending register

corresponding to a highest priority interrupt request to be processed and

providing the bit string to said microprocessor; (col.4, line 43-col.6, line 43),

(col.3, lines 15-61, ie bits stored in pending register are active bits which CPU

determine from interrupt signals 42 or 43(sources) has the highest priority to be

handle by reading the information contained in interrupt flag register provided to

responding to the interrupts.)

said microprocessor identifying and processing an interrupt corresponding

to the highest priority interrupt requested based upon the bit string and the

interrupt command without having to read said interrupt pending. (col.4, line 43-

col.6, line 43), (col.3, lines 15-61, ie bits stored in pending register are active bits

which CPU determine from interrupt signals 42 or 43(sources) has the highest

priority to be handle by reading the information contained in interrupt flag register

provided to responding to the interrupts.)

As per claims 16, 24, Moyer discloses wherein said auxiliary interrupt control

circuit comprises an encoder for generating the bit string based upon a position

of the active bit in the interrupt pending register. (col.6, lines 1-43), (col.4, line 43-

col.6, line 43)

As per claim 17, Moyer discloses the computer system further comprising an auxiliary register coupled to said interrupt pending register for storing a copy of the interrupt requests, and wherein said encoder generates the bit string based upon the interrupt requests stored in said auxiliary register. (col.6, lines 1-43 ie interrupt flag register 62)

As per claims 18,25, Moyer discloses wherein said auxiliary interrupt control circuit further comprises at least one interrupt priority mask circuit coupled to said encoder, and wherein said encoder generates the bit string responsive to said at least one interrupt priority mask circuit. (col.5, line 1-col.6, line 43)

As per claims 19, 26, Moyer discloses wherein said auxiliary interrupt control circuit further comprises a memory coupled to said at least one priority mask circuit for storing interrupt priority values for configuring said at least one priority mask circuit. (col.5, line 1-col.6, line 43)

As per claim 22, Moyer discloses wherein the identified active bit of the highest priority interrupt request is the first active bit in the pending interrupt register. (col.5, line 1-col.6, line 43, ie high order bits s the highest priority)

As per claim 23, Moyer discloses an auxiliary interrupt control circuit, (fig.2, 10 ie data processing system) for use in a computer system comprising at least one

peripheral (fig.2, 50 ie interrupt sources) for generating interrupt requests, an

interrupt pending register (fig.2, 58 ie interrupt pending register) for storing the

interrupt requests, a microprocessor(fig.2, 12 ie cpu) for processing interrupts,

and an interrupt control circuit(fig.2, 81 ie Oring circuit) associated with said

microprocessor, said auxiliary control circuit comprising: (col.4, line 43-col.5, line

47)

an auxiliary register coupled to said priority interrupt register for storing a

copy of the interrupt requests; and(col.4, line 43-col.5, line 47)

an encoder coupled to said auxiliary register and the microprocessor for

generating a bit string identifying an active bit stored in the auxiliary register

corresponding to a highest priority interrupt request to be processed and

providing the bit string to the microprocessor so that the microprocessor identifies

and processes an interrupt corresponding to the highest priority interrupt request

based upon the bit string and an interrupt command without having to read the

interrupt pending register. (col.4, line 43-col.6, line 43), (col.3, lines 15-61, ie bits

stored in pending register are active bits which CPU determine from interrupt

signals 42 or 43(sources) has the highest priority to be handle by reading the

information contained in interrupt flag register provided to responding to the

interrupts.)

As per claim 29, Moyer discloses a peripheral (fig.2, 50 ie interrupt sources) to be coupled to a microprocessor(fig.2, 12 ie cpu) having an associated interrupt control circuit(fig.2, 81 ie Oring circuit), the peripheral comprising:

a peripheral controller for generating interrupt requests; (col.4 line 43-col.5, line 47)

an interrupt pending register(fig.2, 58 ie interrupt pending register) for storing the interrupt requests; and

an auxiliary interrupt control circuit (fig.2, 10 ie data processing system) coupled to said interrupt pending register and the microprocessor for generating a bit string identifying an active bit stored in said interrupt pending register corresponding to a highest priority interrupt request to be processed and providing the bit string to the microprocessor so that the microprocessor identifies and processes an interrupt corresponding to the highest priority interrupt request based upon the bit string and an interrupt command without having to read said interrupt pending register(col.4, line 43-col.6, line 43), (col.3, lines 15-61, ie bits stored in pending register are active bits which CPU determine from interrupt signals 42 or 43(sources) has the highest priority to be handle by reading the information contained in interrupt flag register provided to responding to the interrupts.)

As per claim 34, Moyer discloses a method for processing peripheral interrupts comprising:

generating interrupt requests using at least one peripheral and storing the

interrupt requests in a pending interrupt register; (col.4, line 43-col.6, line 43)

generating a bit string identifying an active bit corresponding to a highest

priority interrupt request in the pending interrupt register to be processed;

and(col.4, line 43-col.6, line 43), (col.3, lines 15-61, ie bits stored in pending

register are active bits which CPU determine from interrupt signals 42 or

43(sources) has the highest priority to be handle by reading the information

contained in interrupt flag register provided to responding to the interrupts.)

identifying and processing an interrupt corresponding to the highest

priority interrupt request based upon the bit string without having to read the

interrupt pending register(col.3, lines 33-39), (col.5, line 1-col.6, line 43, ie high

order bits s the highest priority)

As per claim 35, Moyer discloses wherein the identified active bit of the highest

priority interrupt request is the first active bit in the pending interrupt register.

(col.5, line 1-col.6, line 43, ie high order bits s the highest priority)

As per claim 38, Moyer discloses wherein generating the bit string comprises

copying the interrupt requests from the interrupt pending register to an auxiliary

register and generating the bit string based upon the copied interrupt requests.

(col.6, lines 1-43)

Allowable Subject Matter

3.   Claims 20-21, 27-28, 32-33, 36-37 are objected to as being dependent upon a

rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims.

Applicant's claimed invention is deemed allowable over the prior art of record as

the prior art fails to teach or suggest wherein said auxiliary interrupt control circuit

further generated and provides to said microprocessor a second bit string identifying a

position of a last active bit in said interrupt pending register.

Response to Amendment

4.   Applicant's amendment filed on 9/18/06 have been fully considered but does not

place the application in condition for allowance.

a. Applicant argues that the CPU in Moyer recognizes which interrupt is to be

served or processed by reading the interrupt pending register 58 via the function of the

selection field 90. In contrast, amended independent claims have been amended to

recite that the microprocessor identifies an interrupt corresponding to the highest priority

interrupt request based upon the bit string and the interrupt command without reading

the interrupt pending register. Examiner respectfully disagrees. As Moyer notes at

(col.3, lines 33-39), the CPU 12 recognizes which interrupt is to be served or processed

by reading the interrupt flag register 62 not by reading directly from the pending register

58. Register 62 has two fields, a selection field 90 and an information field 91. The

selection field 90 identifies the source of the information loaded in the information filed

91 and the selection field 90 identifies which of the two registers portions of the interrupt

pending register 58 is loaded into the register 62. This is equivalent to applicant's

claimed languages as "the microprocessor identifies an interrupt corresponding to the

highest priority interrupt request based upon the bit string and the interrupt command

without reading the interrupt pending register". Thus, the prior art teaches the invention

as claimed and the amended claims do not distinguish over the prior art as applied.

Conclusion

5.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

6.   *Any inquiry concerning this communication or earlier communications from the examiner should*

be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to

[kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be

reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].

The fax phone numbers for the organization where this application or proceeding is assigned are

(571)273-8300 for regular communications and After Final communications. Any inquiry of a general

nature or relating to the status of this application or proceeding should be directed to the receptionist

whose telephone number is (571)272-2100.

Kim Huynh

November 22, 2006

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
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